## CLAIMS

1. A digital signal processing method, comprising:

configuring a portion of an array of independently reconfigurable processing elements for performing a turbo coding routine; and

executing the turbo coding routine on data blocks received at the configured portion of the array of processing elements.

2. The method of claim 1, wherein configuring a portion of the array of reconfigurable processing elements includes activating the portion with an activation signal.

3. The method of claim 1, wherein the portion of the array of independently reconfigurable processing elements includes at least one processing element.

4. The method of claim 1, wherein executing the turbo coding routine on data blocks received at the configured portion of the array of processing elements includes encoding the data blocks.

5. The method of claim 1, wherein executing the turbo coding routine on data blocks received at the configured portion of the array of processing elements includes decoding the data blocks.

6. The method of claim 1, wherein configuring a portion of an array of independently reconfigurable processing elements for performing a turbo coding routine includes configuring the portion as a logarithmic maximum a posteriori (LOG-MAP) -based processor.

7. The method of claim 6, further comprising configuring the portion to access a look-up table.

8. The method of claim 1, further comprising idling all processing elements in the array other than the portion of processing elements configured for performing the turbo coding routine.

9. The method of claim 1, wherein each processing element includes at least one functional unit, and wherein configuring a portion of an array of independently reconfigurable processing elements for performing a turbo coding routine includes programming the functional unit to perform at least one function of the turbo coding routine.

10. The method of claim 9, wherein the function unit includes programmable logic that is configurable for performing a logical function.

11. A digital signal processing apparatus, comprising:

an array of interconnected, reconfigurable processing elements, each processing element being independently programmable with a context instruction;

a context memory connected to the array for storing and providing the context instruction to the processing elements; and

a processor connected to the array and to the context memory, for controlling the loading of the context instruction to the processing elements, for configuring a portion the processing elements to perform a turbo coding routine.

12. The apparatus of claim 11, wherein the processor is further configured to execute the turbo coding routine by controlling a state of the configured portion of processing elements.

13. The apparatus of claim 11 wherein the array, the context memory, and the processor reside on a single chip.

14. The apparatus of claim 11, wherein the turbo coding routine is an encoding process on data blocks received at the portion of the array.

15. The apparatus of claim 11, wherein the turbo coding routine is a decoding process on data blocks received at the portion of the array.

16. The apparatus of claim 11, wherein each processing element includes at least one functional unit that is programmable for performing at least one function of the turbo coding routine.

17. The apparatus of claim 16, wherein the functional unit includes programmable logic that is configurable by the context instruction.

18. The apparatus of claim 11, wherein the processor is further configured to idle all processing elements that are not of the portion of processing elements configured for performing the turbo coding routine.

19. The apparatus of claim 11, wherein the context instruction is configured to program the portion of processing elements to emulate a logarithmic maximum a posteriori (LOG-MAP) processor.

20. A digital signal processing apparatus, comprising:

a context memory for storing one or more context instructions for performing a turbo coding routine; and

an array of independently reconfigurable processing elements, each of which is responsive to a context instruction for being configured to execute a portion of the turbo coding routine.